04-09-03

2818

First Named Inventor	Christopher S. Johnson
Serial No.	10/073,543
Filing Date	February 11, 2002
Group Art Unit	2818
Examiner Name	Thong Q. Le
Attorney Docket No.	400.149US01

TRANSMITTAL FORM UNDER 37 CFR 1.10
(LARGE ENTITY)

Title: USER SELECTABLE BANKS FOR DRAM

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

Enclosures

The following documents are enclosed:

X A response to Non-Final Office Action (4 pgs.);
X 2 sheets of redlined drawings;
X A return postcard.

Please charge any additional fees or credit any overpayments to Deposit Account No. 501373.

CUSTOMER NUMBER 27073

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Fee Calculation

	Number of Claims		Prv. Amt.	Extra Claims		Fee		Fee Paid
Total Claims		-20			X	$18	=	$
Independent Claims		-3			X	$84	=	$
							=	
							Total	$

Submitted By

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Certificate of Mailing

"Express Mail" mailing label number: EV256355699US Date of Deposit: April 8, 2003
These papers and fees are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and addressed to the Commissioner for Patents, Washington, D.C. 20231.

(LARGE ENTITY TRANSMITTAL UNDER 37 C.F.R. 1.10)

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RESPONSE TO NON-FINAL OFFICE ACTION

#4 Response
M. Brunn
4/12/03

Title: USER SELECTABLE BANKS FOR DRAM

Commissioner for Patents
Washington, D.C. 20231

In response to the non-final Office Action mailed January 8, 2003, please consider the following remarks.

REMARKS

In the Drawings

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5), as they did not include the following reference sign(s) mentioned in the description: **Bank decoder, Column decoder, Row decoder**. Applicant submits that Figures 1 and 3 clearly show the bank decoder 105, row decoder106, and column decoder 108. They are identified as such in the specification, and appropriately labeled in the Figures. However, Applicant submits herewith proposed drawing corrections to Figures 1, 2, and 3 in redline format, and requests approval of the proposed corrections.

Rejections Under U.S.C. § 112

Claims 2 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant traverses this rejection so far as it is understood. Applicant does not see how claim 2, which recites "four or eight banks" fails to teach "four banks or eight banks." Further, Applicant does not understand what the Office Action finds does not meet 35 U.S.C. § 112, second paragraph, and respectfully requests withdrawal or clarification of the rejection.

Rejections Under 35 U.S.C. § 102

Claims 1-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by Li (U. S. Patent No. 6,044,032). Applicant strongly traverses this rejection, and submits that Li does not show each and every element of the claims as is required for a proper showing under 35 U.S.C. § 102.

Specifically, Li is directed to and discloses an addressing scheme for a double data rate (DDR) memory. The specific features and requirements of Li for addressing that specific type of memory do not contain the elements of the claims. At no place in Li can Applicant find any mention or disclosure of the ability of Li to reconfigure an existing configuration to have a different number of banks. Li does say it can operate its structure with a number of banks other than four, but nowhere does Li allow for the reconfiguration of the existing banks to act as more banks. The division of banks into subsections is not the same as the reconfiguration of banks to act as a different number of banks.

Claim 1 recites "address circuitry coupled to the mode register to configure the addressable banks in response to a program state of the mode register." Col. 4, lines 43-65 of Li makes no showing of any configuration of the mode register configuring the banks in response to a program state of the register. Instead, Li discusses the mode register being able to load information about burst length and type.

Claim 4 recites that "the mode register defines a number of addressable banks of the array." This is neither taught nor disclosed in Li. Applicant cannot find in Figure 2 or 3 where Li discloses the mode register performing any definition of a number of addressable banks. In fact, the number of addressable banks in Li is static. The present claims reconfigure the number of banks without changing the density, whereas Li uses a static number of banks, but can operate with different static numbers. This however, changes density.

Claim 9 recites "a mode register" and "address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data stored in the mode register." Claim 19 recites "logic circuitry coupled to the at least one external input connection" and "address signal circuitry

coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to the logic circuitry." Address circuitry in Li routes address input connections to row decoders or column decoders, as is clearly shown in the Figures, and in the specification. In contrast, the present claims recite the routing of addresses to either the row decoder or the bank address decoder. This difference allows the present claims to decode information provided by the mode register or logic circuitry that is not present in Li, namely the information as to whether the memory is to operate in one or the other of its configurable number of bank modes. Since Li does no reconfiguration or changing of the number of banks, there is no such information presented in Li, and Li therefore does not teach each and every element of claims 9 or 19.

Claims 12 and 16 each recite processes neither taught nor disclosed in Li. The disclosed structure in Li does not perform the method of either of claims 12 or 16. There is no teaching whatsoever in Li of "adjusting address circuitry of the memory device in response to the programmed mode register, wherein the address circuitry configures a number of addressable banks of a memory cell array" as is recited in claim 12 or of "outputting mode register data from a processor to a memory device, wherein the mode register data contains bank count data" or "adjusting address circuitry of the memory device in response to the programmed mode register, wherein the address circuitry configures a number of addressable banks of a memory cell array using the bank count data" as is recited in claim 16. Accordingly, since Li does not teach each and every element of claims 12 and 16, Applicant believes those claims to be allowable.

Further, each memory bank of Li is always divided into at least two planes, which is neither recited nor required by the present claims. In fact, claims 1, 4, 10, 11, 20, and 21 specifically recite the division of the banks in direct contradiction with the teachings of Li, namely that in certain of those recitations, the memory banks are undivided.

Applicant believes claims 1, 4, 9, 12, 16, and 19 are allowable. Claims 2-3, 5-8, 10-11, 13-15, 17-18, and 20-22 depend from and further define patentably distinct claims 1, 4, 9, 12, 16, or 19, and are also believed allowable.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of claims.

The Examiner is invited to contact Applicant's Representatives at direct dial (612) 312-2203 if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

Date: 8 April 2003

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